

Front End Electronics for the Auger Surface Detector Photomultiplier Tubes

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Possible sketch for the Auger Surface Detectors

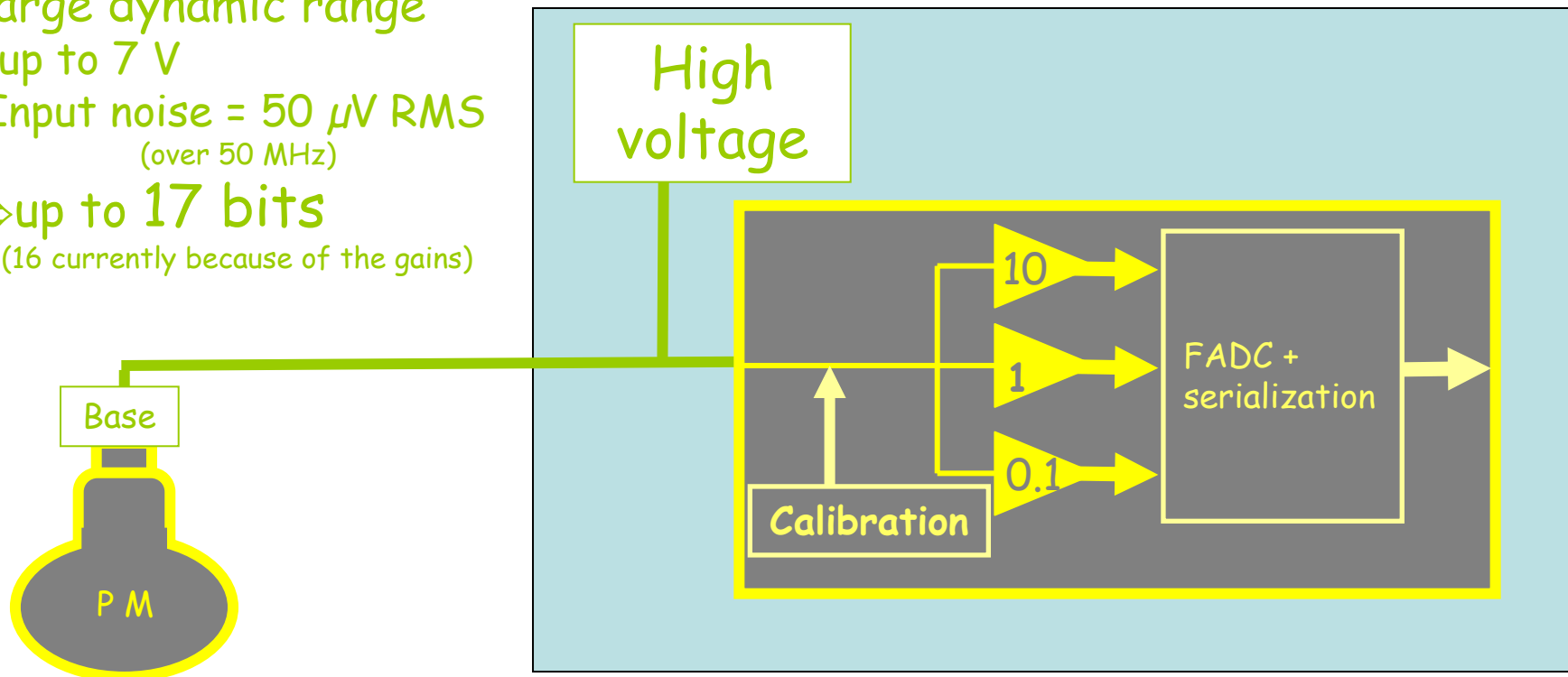
Large dynamic range

- up to 7 V

- Input noise = $50 \mu\text{V RMS}$
(over 50 MHz)

⇒ up to 17 bits

(16 currently because of the gains)



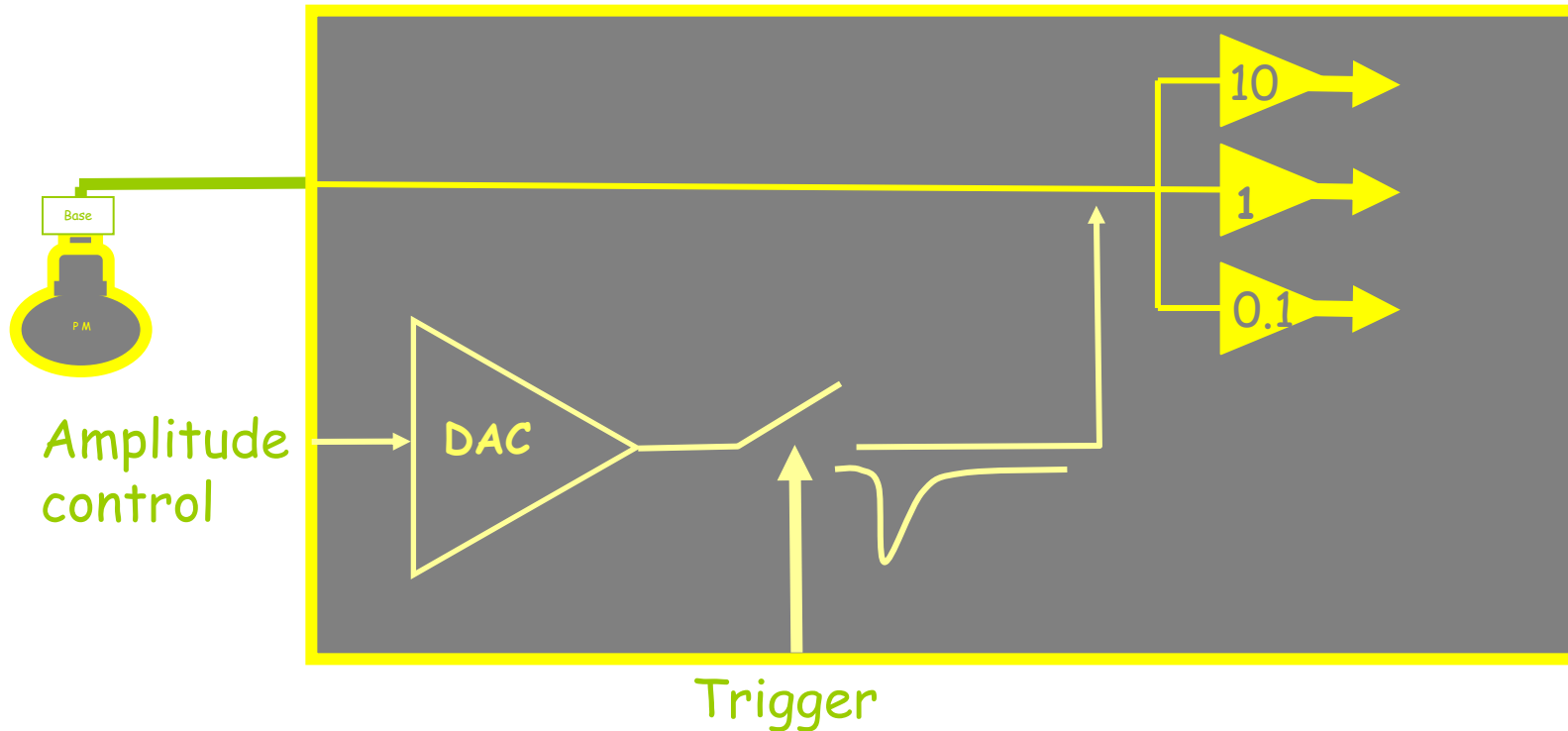
Reduce the number of cables

High voltage and signal through the same cable

75 Ohm impedance

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Calibration principle (current studies)



Adapt ATLAS calorimeter calibration:

Inject muon-like pulses (i.e. with a decay)

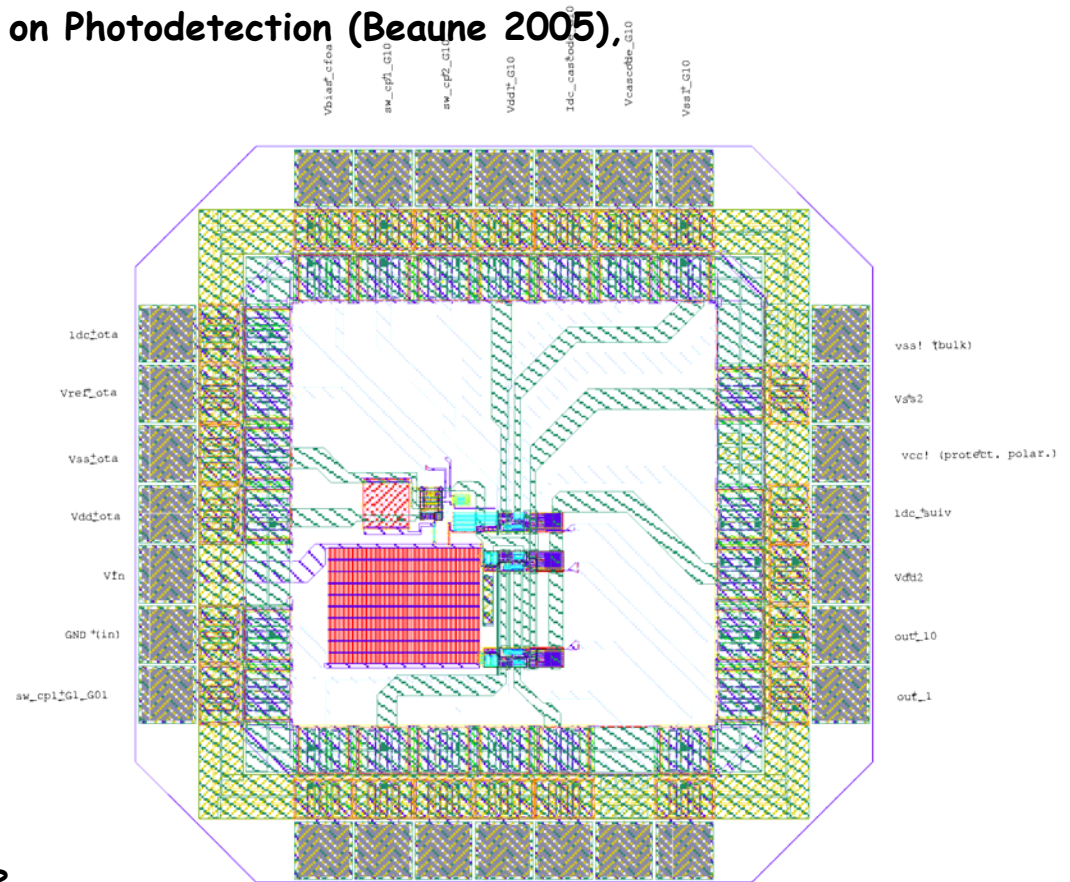
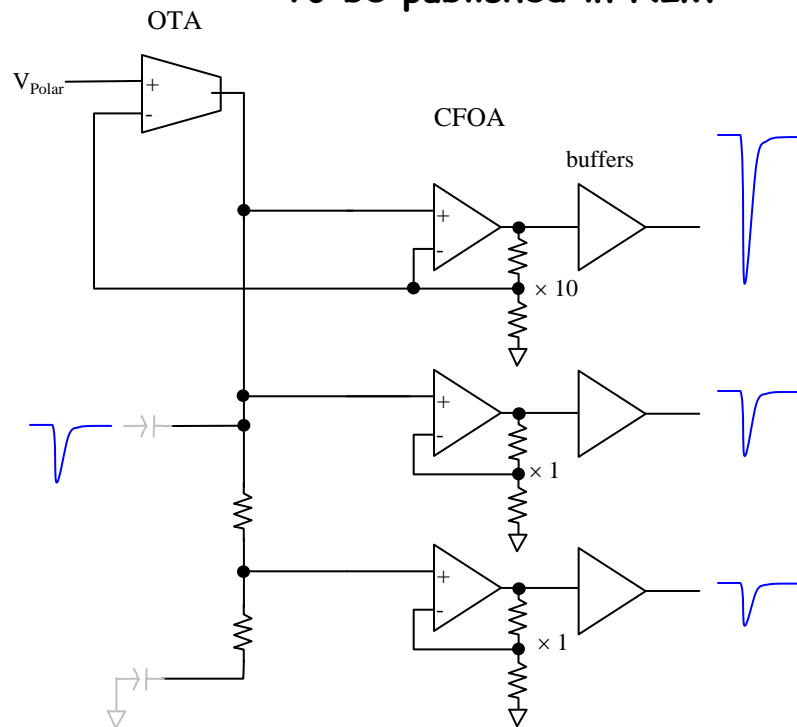
Control the amplitude with the DAC:

⇒ test **linearity** and **gains**

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April 2004 submission

Presented at the Conference on Photodetection (Beaune 2005),
To be published in NIM



Calibration not implemented this time

Pure **0.35 μm CMOS** (AMS) - Size: 1,200 μm \times 1,200 μm

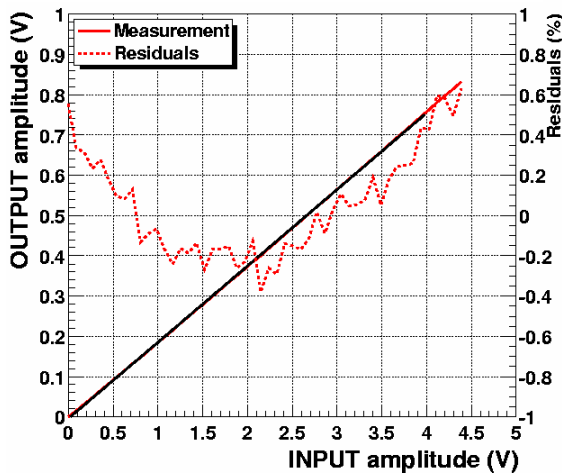
Design based on **CFOA** (current feedback amplifiers), biased with an **OTA** (transimpedance amplifier)

Estimated power absorption: less than 2 mW (<400 μA on 5 V)

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Measurements (Sept. - Oct. 2004)

Gain 0.1



Linearity limit

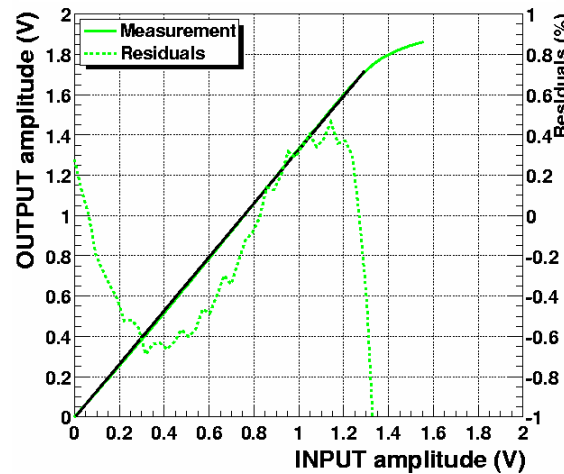
Input: >5 V

Output: > 1 V

Gain 0.2

Noise RMS: 200 μ V

Gain 1



Linearity limit:

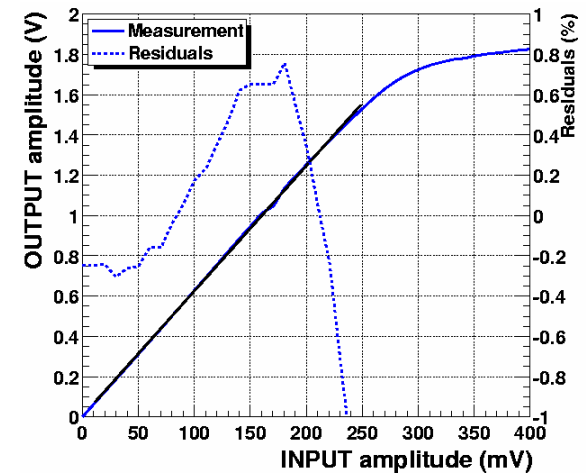
Input: 1.3 V

Output: 1.7 V

Gain 1.3

Noise RMS: 200 μ V

Gain 10



Linearity limit:

Input: 230 mV

Output: 1.4 V

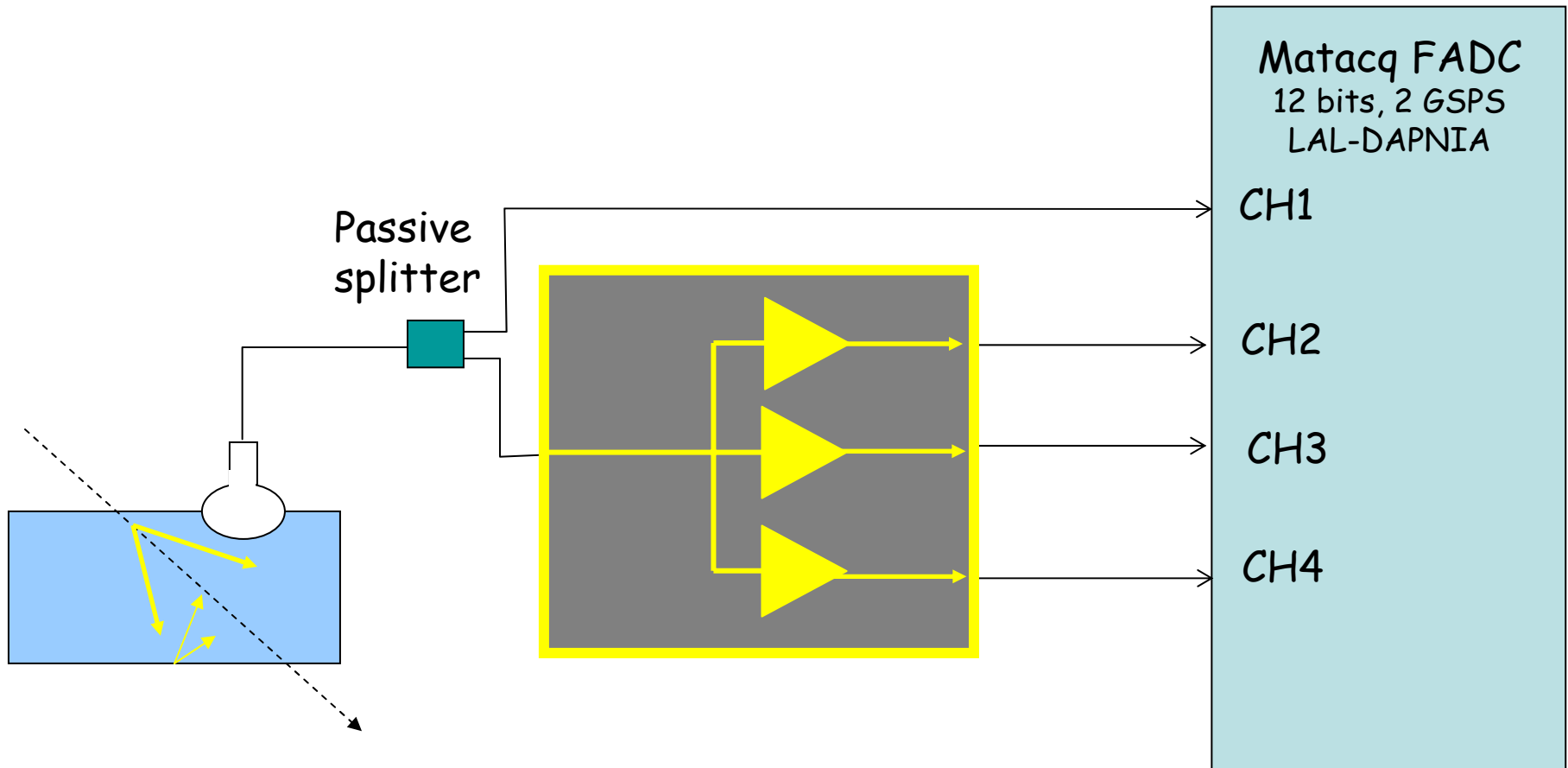
Gain 6.2

Noise RMS: 1200 μ V
Bandwidth = 500 MHz

Linearity better than 1 % over the measured range

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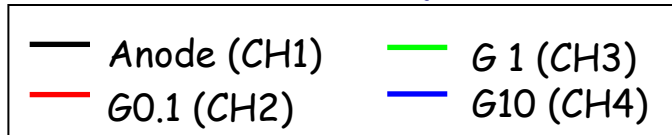
Measurement on the Orsay tank (Oct. 2004)



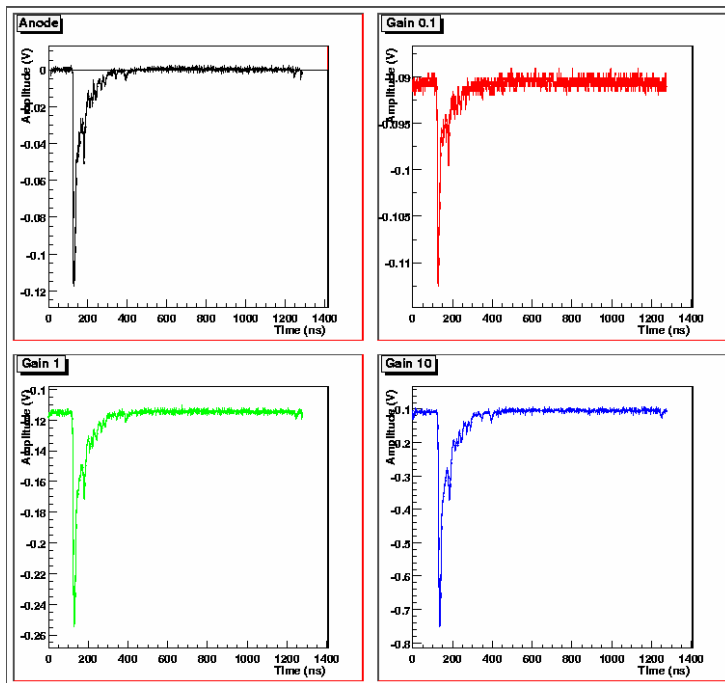
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Measurement: Orsay tank response

PMT gain: around 3×10^6
(to measure greater pulses)

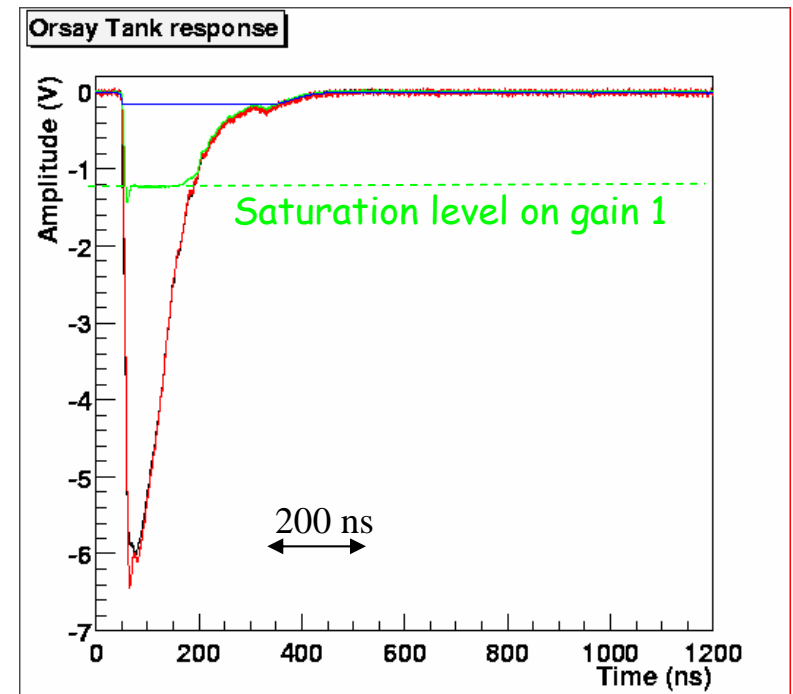


Curves rescaled to the input



Small amplitude
(100 mV input)

Conservation of the signal shape

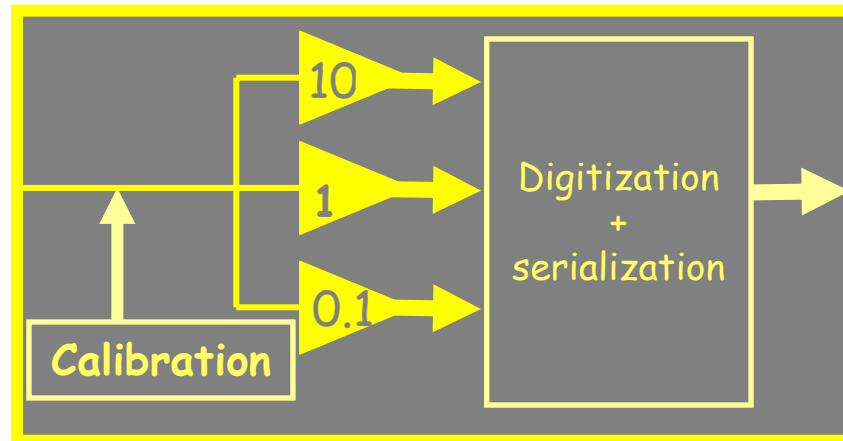


Large amplitude (6V input)
Large width

Fast recovery

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Integrated digitization



Sampling rate: move to 100 MSPS

Output: change to serial

Differential

Electromagnetic compatibility

Serial

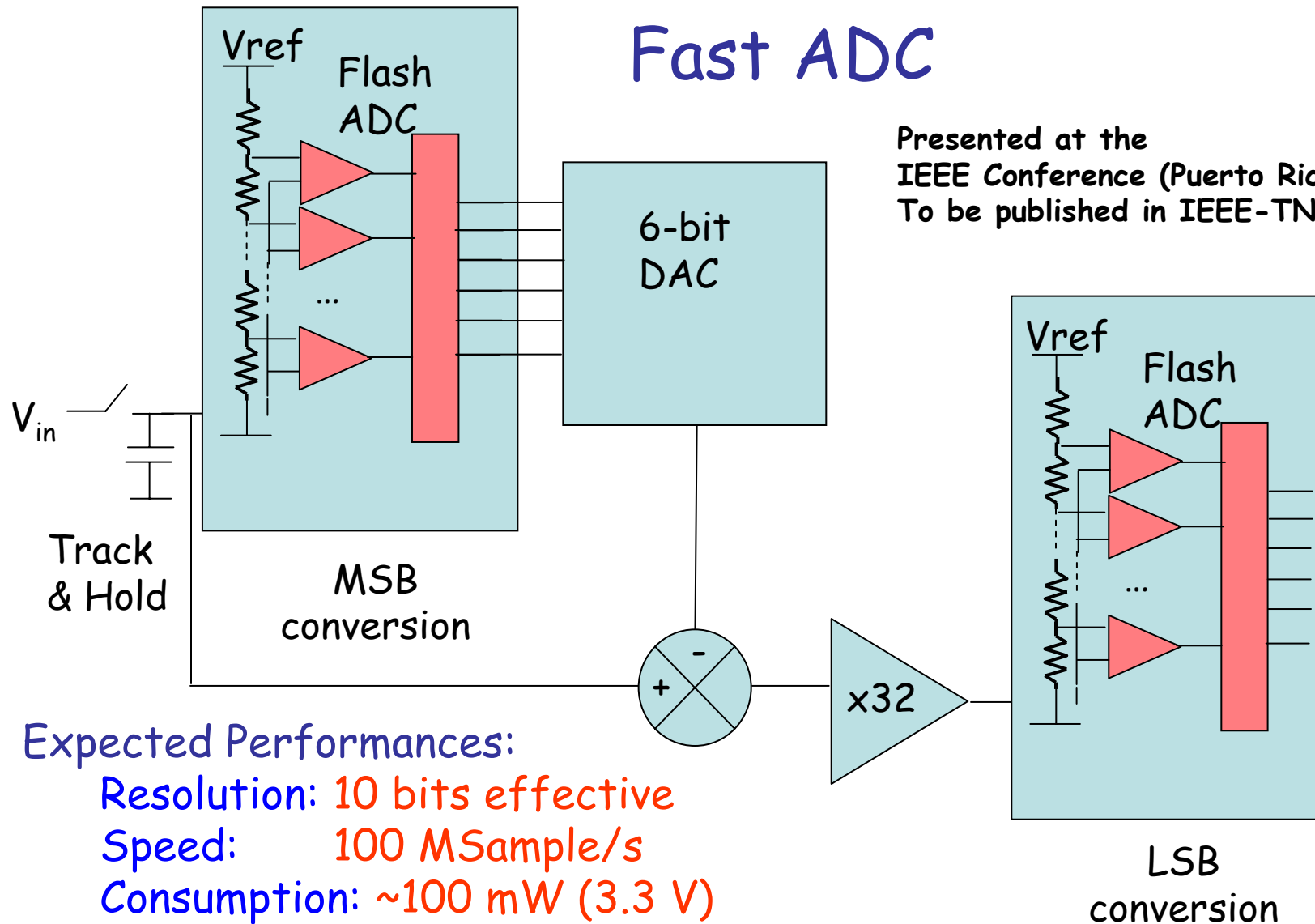
Power (consumption from $di/dt \Rightarrow$ EMC)

Reliability (less pins)

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Fast ADC

Presented at the
IEEE Conference (Puerto Rico 2005),
To be published in IEEE-TNS



Expected Performances:

Resolution: 10 bits effective

Speed: 100 MSample/s

Consumption: ~100 mW (3.3 V)

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Requirements

Analog front-end:

Implement an integrated calibration system (allow a few external components)

Implement a method to match the cable impedance (trimming at production)

Adjust the amplifier gains / increase the bandwidth

Input impedance to 75 Ohms: Better current readout
high voltage coaxial cable

Discriminators:

3 levels, stable levels over the temperature range (-10 to 50°C)

5 ns accuracy

ADC:

10 bits

Sampling time: 100 MSPS (adapted shaping)

Pedestal stability over the temperature range (-10 to 50°C)

Automatic switch mode / dedicated switch mode for calibration

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Our R&D program

November 2003	Beginning of simulations 3 Gains (0.1 ; 1 ; 10) & Calibration
May 2004 -October 2004	Asic submission + tests
October 2004	Start Front-end simulations with extended functions
December, 6 2004	Submission of a 100 MSPS ADC chip (IN2P3 building block) + test board design (prototype of a 10 bit ADC)
August 2005	ADC test
September 2005	Second ADC submission

Then... Tests... Simulations... and

Further submissions in 2006 (front-end, maybe FADC)